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Defects and Impurities in 4H- and 6H-SiC
Homoepitaxial Layers: Identification, Origin,
Effect on Properties of Ohmic Contacts and
Insulating Layers and Reduction

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I. Introduction

The two most important materials-related problems affecting the performance of all SiC devices and their associated components (e.g., contacts) are the defects and the undesired impurities which become incorporated in the homoepitaxial SiC layers in which all devices are currently fabricated. Bhatnagar [1] has shown that the reverse blocking leakage current in high voltage Schottky diodes is three orders of magnitude higher than theoretically predicted as a result of defects in the epi-layer. The formation of micropipes, stepped screw dislocations, interacting dislocation loops, polyganized networks of dislocations and growth twins as well as stacking faults during the sublimation growth of SiC boules are likely the root cause of some of the defects in the epitaxial layer. However, with the exception of the micropipes, the types and concentrations of line, planar and other three-dimensional defects and their effect on the performance of devices and individual device components in the important epi-layer have not been similarly determined. As such, it is not known which of the latter defects actually are translated from the wafer into the epi-layer during its deposition and, therefore, should be vigorously controlled during boule growth and which defects are generated during deposition.

The relatively uncontrolled occurrence of the n-type donor of N and deep level compensating impurities such as Ti in the epilayer have been identified via secondary ion mass spectrometry, photoluminescence and cathodoluminescence investigations. However, the origins of essentially all of these impurities are unknown. For high-temperature, -power and -frequency devices, it is highly desirable to control or eliminate these impurities such as to attain undoped films with uncompensated carrier concentrations of 10^{14} cm^{-3} —two orders of magnitude lower than what is, at present, normally achieved in standard commercial depositions.

The formation of low resistivity and thermally stable ohmic contacts to 4H- and 6H-SiC remains a serious problem in the development of SiC device technology. For SiC power devices to have an advantage over Si, the contact resistivities must be below $1 \times 10^{-5} \text{ W}\cdot\text{cm}^2$, as noted by Alok, *et al.* [2]. In addition, the electrical characterization of state-of-the-art SiC films depends on the ability to fabricate ohmic contacts on material with low carrier concentrations. Therefore, better ohmic contacts are needed both for improving device performance and for improving the quality of films which can be grown. The thermal stability of ohmic contacts is of particular concern for p-type SiC, which have traditionally relied on low melting point Al or Al alloys to dope the SiC surface below the contacts. These materials are not suitable for devices intended for high-temperature operation. While the fabrication of ohmic contacts to SiC has also normally depended on the attainment of a very heavily-doped near-surface region, the introduction during deposition of high levels of dopants in the near surface device region of the epi-layer prior to the deposition of the contact or by ion implantation through the contact makes probable the introduction of point and line defects as a result of the induced strain in the lattice.

Based on all of these issues and recent experiments already performed at NCSU, our goals are to produce contacts which are thermally stable and have low contact resistivities while also reducing the need for doping by ion implantation.

To fabricate most microelectronic devices, the growth or deposition of stable insulators is needed to provide both passivating layers and gate dielectrics. Silicon carbide is almost invariably thermally oxidized, albeit at a slower rate, in the same manner and temperature range that is employed for Si. Most of the previous studies regarding the oxidation of SiC have been concerned with polycrystalline materials. It has been shown by Harris and Call [3] and Suzuki, *et al.* [4] that the (0001) face of 6H-SiC oxidizes according to the same linear-parabolic equation reported for Si by Deal and Grove [5]. The model states that the initial stage of oxidation is reaction rate limited and linear, but becomes parabolic as the diffusion of the oxidant through the oxide becomes the rate limiting factor. Research at NCSU by Palmour, *et al.* [6] has demonstrated that the oxidation process on SiC in wet and dry oxygen and wet argon obeys the linear-parabolic law. Both wet processes had a slower rate than dry oxidation at 1050°C and below. The dry oxides exhibited a very flat surface; in contrast, SEM and TEM revealed that wet oxidation preferentially oxidizes dislocation bands, causing raised lines on the oxide and corresponding grooves in the SiC. It was proposed that the much higher solubility of H₂O in SiO₂ as compared to that of O₂ allows wet oxidation to be preferential.

All of the oxidation studies on all polytypes of semiconductor quality SiC have been conducted on n-type material with the exception of the investigation by Palmour *et al.* [6]. The objective of this study was the determination of the redistribution of the common electrical dopants of N, P, Al and B during thermal oxidation of SiC films at 1200°C in dry O₂. Experimental segregation coefficients and interfacial concentration ratios were determined. Secondary ion mass spectrometry revealed that B and Al depleted from the SiC into the growing oxide while N and P were found to pile up in the SiC as a result of the loss of the SiC to the oxide formation. Aluminum is now used almost universally as the p-type dopant in SiC. The electrical properties of oxides thermally grown on n-type SiC normally have reasonably favorable characteristics of high breakdown voltage and low leakage currents. However, the reverse is true for thermally grown oxides on p-type SiC, as shown by Baliga and his students at NCSU. It is believed that at least two of the causes of the poor performance on a p-type material are the existence of the Al in the oxide and at the oxide/SiC interface and the dangling oxygen bonds which this species creates in the oxide as a result of a difference in oxidation state (+3) compared to that of Si (+4) and the existence of C at the SiC/insulator interface. Methods of effectively cleaning SiC surfaces prior to oxidation to deposit and grow oxides on p-type material under UHV conditions and determine the effect of Al redistribution and C concentrations at the interface on the properties of the oxide must be determined. In addition,

the effect of existing line and planar defects in the SiC epi-layer on the properties of the thermally grown and deposited oxide must be ascertained.

The research conducted in this reporting period and described in the following sections has been concerned with the (1) design and construction of a new hot wall CVD SiC system for the deposition and doping of 6H- and 4H-SiC and AlN films, (2) the fabrication and characterization of MOS capacitors and MOSFET devices, (3) the deposition and characterization of AlN films as new insulators for SiC devices, and (4) the morphology of silicon oxides on silicon carbide. The following individual sections detail the procedures, results, discussions of these results, conclusions and plans for future research. Each subsection is self-contained with its own figures, tables and references.

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II. Growth Via Hot Wall Chemical Vapor Deposition and Characterization of 6H- and 4H-SiC Thin Films

A. Description of Equipment

The system design is comprised of a six way cross, serving as a loadlock, from which two separate chambers are attached. A high temperature growth chamber and RHEED analysis chamber are attached on each side perpendicular to the axis of the loadlock. The latter chamber will be used to monitor film crystallinity, crystal structure and the formation of new surfaces. The sample will be transferred to and from the various chambers on a SiC coated graphite susceptor platform on which the sample will be placed. The transfer mechanism consists of a platform which is moved from chamber to chamber by means of a manipulator rod which is fastened to the side of the susceptor.

The growth chamber consists of a rotating module, to which the susceptor is attached. Growth will occur on the sample in an upside-down position, with gases flowing upward, while the susceptor is being rotated. The susceptor is attached to the rotating rod assembly by a groove into which the susceptor slides when transfer of the sample takes place. Once the sample is transferred to the rotating rod, the rod is brought down to the quartz portion of the reaction chamber. Here, the sample is heated via RF coil, and gases are introduced from the bottom of the reactor. A design which incorporates a graphite cylinder for hot wall CVD growth is in progress. The growth temperature will be monitored by means of a standing pyrometer mounted outside the quartz chamber and aimed at the sample. Growth processes parameters, such as gas flow rate and pressure, will be monitored by electronic components. Gas flow will be controlled by mass flow controllers and pressure by capacitance manometers.

The SiC growth process will consist of introducing SiH₄ and C₂H₄ as the reactive components in a H₂ carrier. Nominal flow values will be on the order of 1 to 10 sccm for each. Hydrogen carrier flow rates will be on the order of three liters per minute. Other reactant sources which will be attached to the system include NH₃ and an N₂/H₂ mixture for n-type doping and triethylaluminum for p-type doping.

B. Accomplishments to Date

- Design and construction of a SiC thin film growth system containing a load lock, growth chamber, RHEED analysis chamber and support frames.
- Three six-way crosses have been assembled with the adjoining gate valves on the frame, and available flanges and window ports have been attached.
- A quartz chamber-to-cross assembly has been machined which will provide a sealed interface between two parts of the growth chamber.
- Quartz cylinders have been cut to design dimensions.

- Flange parts, pressure gauge attachments, pump connection parts, and a rotating rod assembly, have been machined.
- An RF generator has been refurbished and returned and will be used to provide RF heating to the susceptor.
- Assembly of a switch panel to control the nupro valves and to enable computer control is complete.
- A RHEED chamber manipulator has being fitted with a holder which will accommodate the susceptor upon transfer.
- Electrical wiring of the switch panel to control the nupro valves has been assembled.
- Assembly of various gas lines on a panel to be mounted on one side of the system has been completed.
- Installation of electrical and water utilities for the system as well as safety changes in the laboratory are being performed at this time.
- A gas monitoring system is being installed for safe system operation.

C. Discussion

The proposed design was developed with many sources of input. A number of constraints determined the design configuration and materials used in the system.

One of the main concerns was the high operating temperature of the growth chamber. Temperatures of approximately 1600-1700°C will be used to grow the SiC films. Quartz was determined to be the best material for the growth portion of the chamber. A double-walled quartz vessel, water cooled around the perimeter, has been designed and constructed for optimum cooling. Discussions are underway at this time regarding the design of the most appropriate graphite inner chamber to place inside the quartz cylinders for achieving a SiC high growth rate.

Another concern was the transfer mechanism of the susceptor and the placement of samples on the susceptor surface. It was decided that small silicon carbide screws would be the most flexible for our purposes to accommodate various sized samples. For the transfer mechanism, a simple tongue-in-groove assembly, moved between chambers by means of a transfer arm which would screw into the side of the susceptor was deemed simplest and most practical.

D. Conclusions/Future Research Plans and Goals

A system design for the deposition of SiC thin films has been developed. Essentially all components have been designed or received. Other needed parts are currently being machined. A graphite inner chamber is being devised to accommodate hot wall CVD growth. The final assembly of the system will be conducted when electrical and water sources to the laboratory are in place.

III. Characterization of Oxides on N- and P-type 4H and 6H-SiC

A. Introduction

Silicon carbide (SiC) has been shown to be an excellent material for the fabrication of devices for high-power, high-frequency and high-temperature applications [1]. The advantages of SiC metal oxide semiconductor field effect transistors (MOSFETs) has also been discussed [2]. The successful operation of these devices hinges on the interface and bulk properties of the gate dielectric, usually an oxide. Previous researchers have reported results on thermally grown oxides on N-type [3-6] and P-type 6H-SiC [5,7-11]. While the results obtained on N-type 6H-SiC have shown that those oxides are of high quality, oxides grown on P-type 6H-SiC exhibit large flatband voltage shifts and are, thus, unsatisfactory for application as gate dielectrics. Oxides deposited under special conditions with surface preparation specific to the particular deposition might show improved interfacial properties over thermally grown oxides. In the recently concluded International Conference on Silicon Carbide and III-Nitrides held in Stockholm, we presented the highest measured inversion layer electron mobility to date in 6H-SiC and further, presented lateral MOSFETs on 4H-SiC for the first time [12]. In this quarter, we successfully reproduced the process obtaining high inversion layer mobilities on both 6H-SiC and 4H-SiC using a deposited annealed gate oxide.

B. Experimental Procedures

The 6H-SiC and 4H-SiC wafers (wafers #1,2 were 6H-SiC and wafers #3,4 were 4H-SiC) used in the experiment were aluminum doped P-type substrates (doping $\sim 10^{18} \text{ cm}^{-3}$) with 2 μm thick aluminum doped P-type epitaxial layers (nominal doping = $1\times 10^{16} \text{ cm}^{-3}$). After an RCA clean without a subsequent buffered HF dip, the wafers were subjected to a sacrificial dry-wet-dry pyrogenic oxidation cycle at 1050°C for 5-240-5 minutes. The resultant 220A was removed using a buffered HF dip. A low temperature oxide (LTO) about 7000A thick was deposited on the wafers at 410°C. The chamber pressure was 750 milliTorr and the gas flow-rates were O₂ at 150 sccm and LTO-410 (disilane) at 75 sccm. This field oxide was then patterned to define the regions receiving the drain-source implants. A further 1000A of LTO was deposited on the wafers under identical conditions to act as pad oxide during the implant. The wafers were then subjected to multiple energy ($1\times 10^{15} \text{ cm}^{-2}$:40keV: $2\times 10^{15} \text{ cm}^{-2}$:80keV) high dose nitrogen implants at 1000°C to obtain the drain-source regions. The wafers were then diced into halves (1A,1B,2A,2B;3A,3B,4A,4B). Wafers 1A and 3A underwent Split 1 which was a control split identical to the process used previously where the gate oxide after being subjected to the 1250°C 30 minute Ar implant activation was then subjected to a wet oxidation cycle (N₂ bubbled through de-ionized (DI) water at 95°C) at 1100°C for 400 minutes followed by an in-situ argon anneal for 60 minutes at 1100°C. The wafers were then ramped

down to 950°C where a re-oxidation anneal was performed using wet N₂ for 60 minutes. This annealing cycle has been reported to greatly improve the interface [13]. Wafers 1B and 3B underwent Split 2 where the gate oxide after being subjected to the 1250°C 30 minute Ar implant activation was then subjected to a wet oxidation cycle (N₂ bubbled through de-ionized (DI) water at 95°C) at 1100°C for 60 minutes followed by an *in situ* argon anneal for 60 minutes at 1100°C. The wafers were then ramped down to 950°C where a re-oxidation anneal was performed using wet N₂ for 60 minutes. This was expected to grow the same thickness of thermal oxide under the thinner gate oxide of the present process than the 400 minute oxidation cycle had done for the thicker gate oxide of the previous process. Wafers 2A and 4A underwent Split 3 where the gate oxide after being subjected to the 1250°C 30 minute Ar implant activation was **not** subjected to any wet oxidation cycle at 1100°C but directly to an argon anneal for 60 minutes at 1100°C. The wafers were then ramped down to 950°C where a re-oxidation anneal was performed using wet N₂ for 60 minutes. Wafers 2B and 4B underwent Split 4 where the gate oxide was **not** subjected to the 1250°C argon activation anneal. Instead this anneal was performed on these wafers before defining the active area and the gate oxide deposited afterwards. The gate oxide was subjected to a wet oxidation cycle (N₂ bubbled through de-ionized (DI) water at 95°C) at 1100°C for 60 minutes followed by an *in situ* argon anneal for 60 minutes at 1100°C. The wafers were then ramped down to 950°C where a re-oxidation anneal was performed using wet N₂ for 60 minutes. Polysilicon was then deposited on the wafers at 550°C for 40 minutes and this was then doped with phosphorus in a furnace using phosphorus disks at 875°C for 180 minutes. The polysilicon was patterned to define the gates and aluminum contacts were provided to the gate, drain and source as well as the SiC substrate on the backside of the wafer. No post-metallizing anneal was done.

C. Measurements

Quasistatic and 100kHz capacitance-voltage (C-V) measurements were performed on MOS capacitors on the wafers using a Keithley Model 82 simultaneous system. Current-voltage (I-V) measurements were made on the FETs using a Keithley Model 251 test system. The accumulation capacitances measured indicated oxide thicknesses in the range of 700-900Å with the variation being mainly from wafer to wafer. The variation was less than 10% across a wafer. The C-V measurements on MOS capacitors showed an average effective charge density N_{eff} of 5×10^{11} - 1×10^{12} cm⁻² (Figs. 1 and 2). The I-V output characteristics of a typical 6H-SiC MOSFET (W/L=160μm/80μm) at 300K up to a gate bias of 50V are shown in Fig. 3. The device exhibits excellent gate controlled linear and saturation regimes of operation. The measured output characteristics of a typical 4H-SiC MOSFET (W/L=160μm/80μm) at 300K up to a gate bias of 50V are shown in Fig. 4. The excellent gate controlled linear and saturation regimes of operation indicate a successful reproduction of lateral MOSFETs on 4H-SiC with

high inversion layer mobilities. The threshold voltage for all MOSFETs was determined from the intercept on the gate bias axis made by the tangent to the transfer characteristics of the MOSFET at the point of inflection. The threshold voltage was measured to be between 2-5V for all measured 4H-SiC and 6H-SiC FETs.

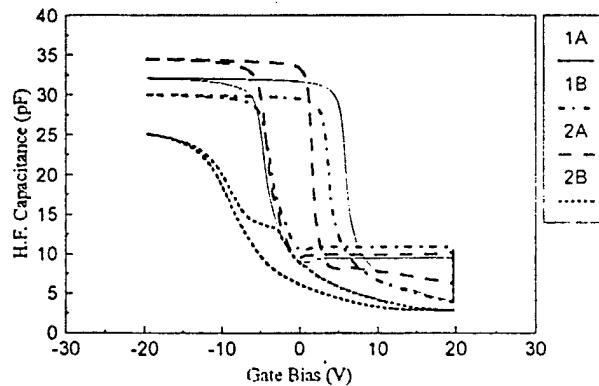


Figure 1. C-V characteristics of MOS capacitors on 6H-SiC with deposited oxide as gate dielectric at 25°C.

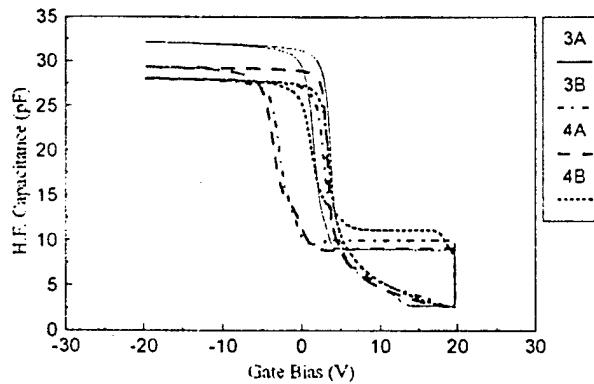


Figure 2. C-V characteristics of MOS capacitors on 4H-SiC with deposited oxide as gate dielectric at 25°C

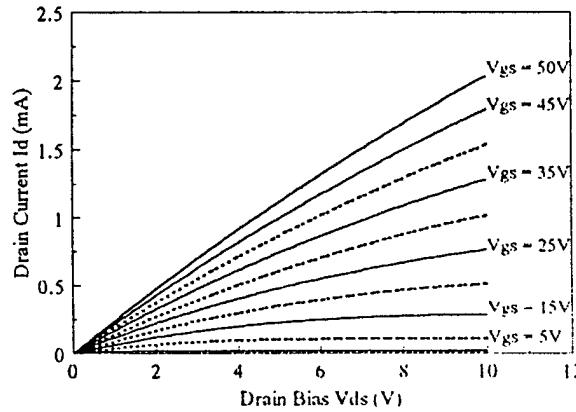


Figure 3. Output characteristics of a 6H-SiC lateral MOSFET ($W/L = 160\mu\text{m}/80\mu\text{m}$) with deposited oxide as gate dielectric at 25°C.

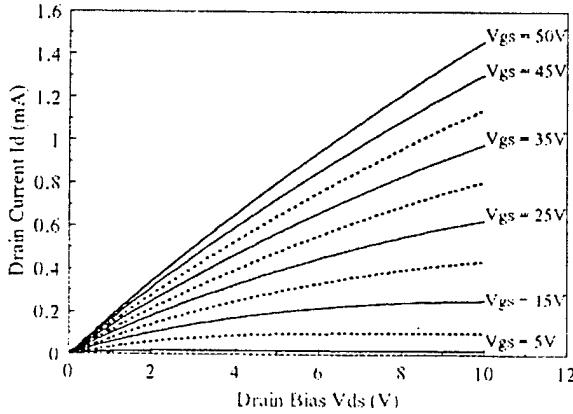


Figure 4. Output characteristics of a 4H-SiC lateral MOSFET ($W/L = 160\mu\text{m}/80\mu\text{m}$) with deposited oxide as gate dielectric at 25°C .

The maximum inversion layer mobility of $60 \text{ cm}^2/\text{V}\cdot\text{s}$ for the 4H-SiC MOSFETs and a maximum inversion layer mobility of $72 \text{ cm}^2/\text{V}\cdot\text{s}$ for the 6H-SiC MOSFETs was extracted from the linear region of the output characteristics (drain bias $V_{DS} = 100\text{mV}$) based on the Eq. 1:

$$\mu_n = \frac{\frac{\partial I_D}{\partial V_{DS}}}{C_{ox} \frac{W}{L} (V_{GS} - V_{th})} \quad 1$$

D. Conclusions

The reproduction of the successful fabrication of lateral high inversion layer mobility MOSFETs on both 6H-SiC and 4H-SiC using a gate dielectric comprising an appropriately annealed LPCVD oxide indicates that the concept is viable. The simplicity of the process is also advantageous for high volume production.

E. Future Research Plans and Goals

During this run, MOSFETs were laid out in different orientations within the c plane. The dependence of inversion layer mobility on this orientation as well as the temperature dependence and the high field dependence of the inversion layer mobility will be characterized.

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IV. Growth of Aluminum Nitride by Gas-source Molecular Beam Epitaxy

A. Introduction

Due to its low dielectric constant and close lattice match to SiC, AlN may be an alternative to silicon dioxide (SiO_2) as a dielectric in high-power and high-temperature SiC devices. Highly (0001)-oriented AlN has earlier been fabricated using reactive magnetron sputtering [1,2], gas-source molecular beam epitaxy (GSMBE) [3], chemical vapor deposition (CVD) [4], and "hot wall" CVD [5]. However, the material contains high densities of line defects and high concentrations of oxygen and carbon. It is also important to reduce the surface roughness of the AlN. This report presents our most recent results [6,7] concerning the growth of AlN by GSMBE using NH_3 as the nitrogen source. It is shown that highly c-axis oriented wurtzite AlN films with very smooth surfaces can be grown on 4H and 6H-SiC substrates.

B. Experimental Procedure

The growth was conducted in a GSMBE system with an ultimate base pressure of 10^{-10} Torr. Prior to growth, SiC substrates were cleaned using procedures developed in the group [3]. The SiC films were grown using SiH_4 and C_2H_4 where the gas-flows were accurately controlled by regulating the pressure over a flow-cell. The AlN growth was made by evaporating Al from an effusion cell and simultaneously introducing NH_3 through a mass flow controller. In addition to the gases mentioned above, it was also possible to introduce H_2 , N_2 and Ar during growth. The system was equipped with two *in situ* analysis tools. The gases in the chamber were monitored with a 100 AMU residual gas analyzer (RGA). Differential pumping of the RGA made it possible to record the gas content in the chamber at pressures above 1×10^{-3} Torr. The surface structures were analyzed with reflection high energy electron diffraction (RHEED).

In addition to these *in situ* techniques several *ex-situ* analysis techniques were available, for instance, transmission electron microscopy (TEM), x-ray diffraction (XRD), scanning electron microscopy (SEM) and atomic force microscopy (AFM) for structural investigations, Auger electron spectroscopy (AES) and secondary ion mass spectroscopy (SIMS) for chemical analysis.

C. Results and Discussion

The RHEED patterns from the AlN surfaces indicated that very smooth films were grown on all types of SiC substrates. This was particularly true for the films grown on the on-axis 4H-SiC(0001), 4H-SiC(000 $\bar{1}$), and 6H-SiC(0001) substrates (Fig. 1). The patterns were very streaked and showed Kikuchi lines. Along $<1\bar{1}00>$, additional streaks were seen due to reconstruction of the AlN surface which also implied that the films had very smooth surfaces.

The RHEED pattern can be interpreted as a $(\sqrt{3} \times \sqrt{3})R30^\circ$ reconstruction. The two reconstruction streaks observed only in the $\langle 1\bar{1}00 \rangle$ pattern were also typical for growth on the vicinal surfaces and C-faced on-axis surfaces. In some cases, however, additional weak reconstruction streaks were seen in the $\langle 1\bar{1}00 \rangle$ patterns indicating some other type of reconstruction. Another possibility is that the $(\sqrt{3} \times \sqrt{3})R30^\circ$ reconstruction coexists with a second type of reconstruction. Reconstructed AlN surfaces were, to the author's best knowledge, reported for the first time [6,7].

Measurements via AFM confirmed that the AlN surfaces were smooth (Fig. 2). The root mean square (RMS) value of the surface roughness were between 0.5 nm and 1 nm for all

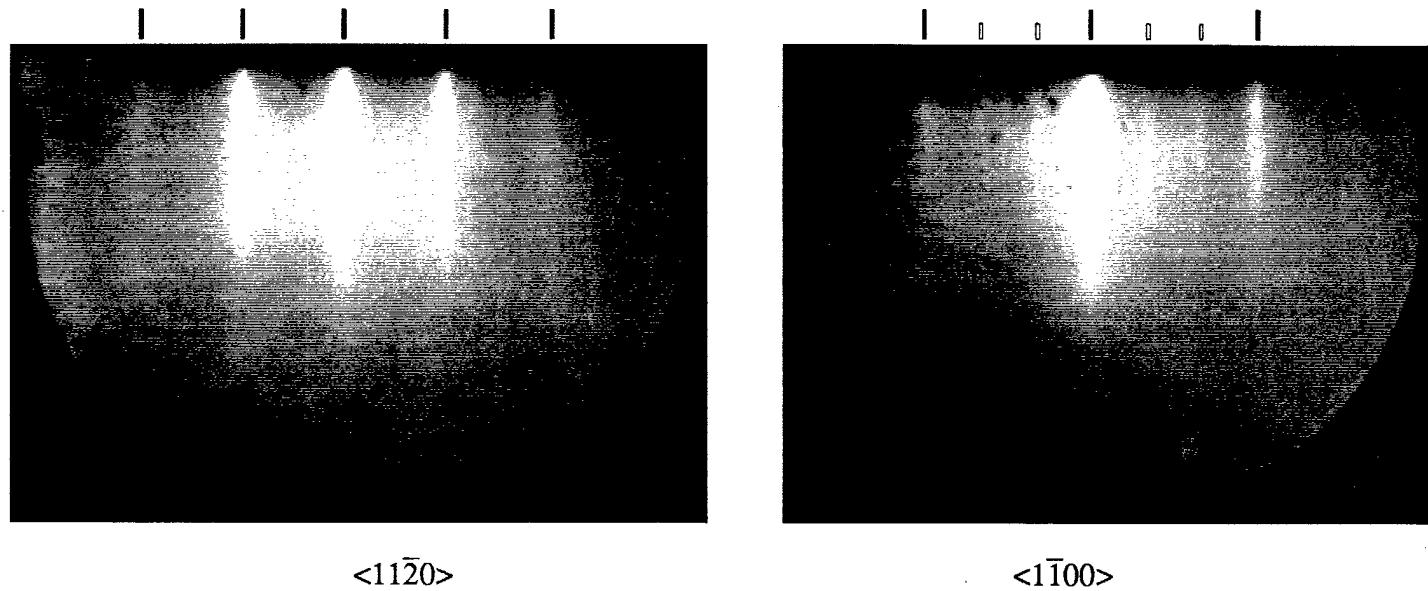


Figure 1. RHEED patterns from an AlN film grown on an on-axis 4H-SiC(0001) substrate. The electron beam was directed along the $\langle 11\bar{2}0 \rangle$ and $\langle 1\bar{1}00 \rangle$ directions of the substrate. Reconstruction streaks were observed in the $\langle 1\bar{1}00 \rangle$ pattern.

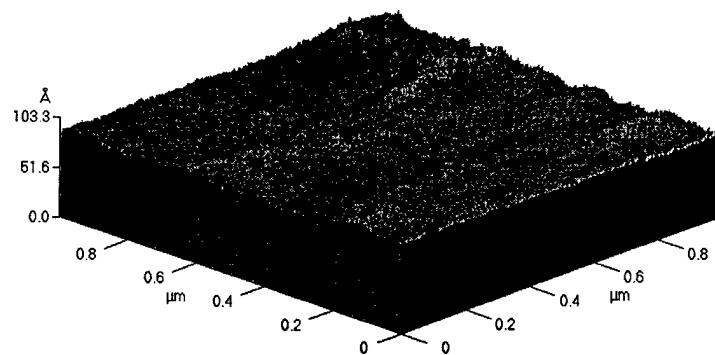


Figure 2. AFM image of an AlN film grown on a vicinal 4H-SiC(0001) substrate. The RMS values of the surface roughness were between 0.5 and 1 nm for all scans on this sample.

measured samples in this work. Cross-sections of the samples investigated by TEM showed very flat surfaces in agreement with the RHEED and AFM results. The films had threading defects can be inversion domain boundaries (IDBs) or stacking mismatch boundaries (SMBs). A highly c-axis oriented structure and no secondary phases were observed using XRD. SIMS measurements of the levels of oxygen, carbon and silicon showed that the concentration of all these materials were high. For instance, the lowest concentration of oxygen in the GSMBE grown films were $\sim 10^{19} \text{ cm}^{-3}$.

D. Future Research Plans and Goals

Presently the RHEED, RGA, TEM, XRD, and SIMS data from the AlN films are analyzed. This will result in a more detailed report [8] regarding the GSMBE growth of AlN.

The previous research [9-11] on GSMBE deposition of SiC on 6H-SiC substrates will be continued. Investigations regarding the mechanisms controlling the surface chemical effects of H₂ on SiC growth rate and polytype change (3C to 6H) will be investigated in more detail. The experiments will also be conducted on 4H-SiC substrates. A goal in this research is to investigate the possibilities to deposit 6H or 4H-SiC on 3C-SiC and wurtzite AlN. Recently the growth system has been slightly modified and is now prepared for SiC growth.

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V. Morphology of Silicon Oxides on Silicon Carbide

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Abstract

The development of high power devices based on silicon carbide requires a more complete understanding of the oxide formation process and interface characteristics. By using an integrated UHV system, samples were cleaned and oxides deposited *in situ*. The approach of the oxide formation process was to form the initial insulator, a few angstroms thick, and then deposit an oxide. Various deposition techniques are used in the oxide growth process; both thermal and plasma enhanced chemical vapor deposition were employed with two different precursors (oxygen and nitrous oxide), and the results were compared with thermal oxidation. The morphology of each of the deposited oxides was compared to the bare substrate and the thermal oxide wafers. This study focuses on the morphology of the different deposition processes using AFM. Examination of the morphology of the initial insulator growth process and the oxide deposition process gives insight into the physical characteristics of the silicon dioxide deposited on silicon carbide. The RMS values of the initial insulator formation and the control wafers are 0.93 and 0.95 nm respectively. Meanwhile, the RMS values for PECVD (200-400°C) and thermal CVD (400-600°C for oxygen-silane and 800-1000°C for nitrous oxide-silane) range from 1.43 to 1.93 nm.

A. Introduction

Wide band gap semiconductors are increasingly being considered in semiconductor applications that require high temperatures and high breakdown characteristics. With the improvement and availability of SiC wafers, the material is now considered to be most promising material for high power semiconductor applications. Another advantage of SiC over other compound semiconductors is that it has a native oxide. However, significant problems persist with the thermal oxidation of p-type SiC. The dopant in p-type SiC (B or Al) is incorporated into the grown oxide, generating traps and fixed oxide charge [1,2]. Because of this phenomenon, there is a need to develop new processes for preparing gate dielectrics. Our approach is to circumvent the problem of dopant redistribution by using deposited oxides as a gate dielectric. The morphology of these deposited oxides becomes a matter for concern. In this study, the morphology of the deposited oxides is compared to that of thermally grown oxides to determine if the deposited oxides are a viable alternative to thermal oxidation for gate dielectric applications.

B. Experiment

The substrates used were partial wafers of p-type 4H-SiC 8 off axis with a 4.5 m epitaxial layer supplied by Cree Research Inc. The samples were wet chemically cleaned using a SC1 etch (5:1:1 H₂O:NH₄OH:H₂O₂) at 80C for 10 min followed by 5 min DI water rinse, and then a SC2 etch (5:1:1 H₂O:HCl:H₂O₂) at 80C for 10 min followed by 5 min DI water rinse [3,4]. The final wet chemical step was a series of UV/Ozone exposures followed by 10:1 HF dips. Samples were then divided into two batches. The first batch was processed in quartz tube furnaces, while the second was processed in a UHV oxide deposition system. Samples processed in the UHV oxide deposition system had tungsten sputtered on the backside using an argon sputterer. The tungsten deposited on the backside acted as an absorber for radiative heating. All samples were then cleaned using a UV/Ozone exposure followed by a 10:1 HF dip. Atomic force microscopy (AFM) was then performed on a series of samples to obtain an overall view of the surface roughness before oxide deposition. After the AFM measurements, all samples were cleaned with a UV/ozone exposure to remove any surface contaminants due to ambient exposure. The samples were then dipped in 10:1 HF and exposed to a buffered oxide etch (BOE) vapor. By holding the sample a few millimeters above a solution of BOE for several minutes the BOE vapor treatment decreases the surface carbon contamination, and increases the fluorine adsorption on the surface. This is a desired quality since the fluorine populates some sites that residual oxygen would populate and it is readily desorbed at low temperatures.

Samples with tungsten on the backside were loaded into a UHV transfer mechanism (base pressure of 1×10^{-9} Torr) which has a series of stations for cleaning, analysis, and oxide deposition. The samples were then cleaned in a hydrogen plasma system (base pressure of 1×10^{-9} Torr) which has been shown to remove surface organics and hydrocarbons [5]. Auger analysis before and after hydrogen plasma cleaning showed residual oxygen on the surface. The residual oxygen was not removed for this study. Likewise, the loaded samples exhibited no LEED pattern for moderate beam energies (<250 eV) while the hydrogen plasma cleaned samples exhibit a sharp 1x1 LEED pattern at low beam energies (<50 eV). The samples were then transferred into the oxide deposition system (base pressure 1×10^{-8}). A tungsten coil radiative heater below the sample was used to heat the substrate. In the oxide deposition system, a variety of processes may be used to deposit oxides. PECVD oxides were deposited by exciting O₂ or N₂O in a quartz tube located 10 cm above the sample with a 13.56MHz RF generator. 1% SiH₄ in hydrogen is introduced just above the sample and not excited in the plasma [6]. Oxide thicknesses of approximately 400Å were deposited in 5 min. LPCVD oxides were also deposited in the oxide deposition system. These were deposited using O₂ and 1% SiH₄ in hydrogen at 550° for 60 min or N₂O and 1% SiH₄ in hydrogen at 750° for 40 min [7]. The samples were then removed and some were selected for annealing in a rapid thermal

annealer (RTA) at 1000°C for 60 sec to densify the deposited oxides. Others were used to obtain the morphology of the PECVD and LPCVD oxides.

Samples that were processed in the quartz tube furnaces did not have tungsten deposited on the backside to avoid contamination of the furnaces. The substrates were again divided into two subsets. A 450Å thick low temperature oxide (LTO) was deposited on the first subset of substrates. The oxide was deposited at 400C using diethylsilane (LTO-410) and oxygen precursors. This deposition system is a horizontal, low pressure CVD system in which the SiC substrate lies flat. After the oxide deposition a set of samples was selected for annealing using a RTA at 1000°C for 60 sec. The second subset of substrates was thermally oxidized at 1 ATM. in pyrogenic steam at 1050°C for 120 min. Following the deposition, the wafers were subjected to a post oxidation anneal at 900°C in N₂ for 60 min [8]. The thermal oxidation was completed in a horizontal Tytan II three-zone furnace in which the SiC substrate lies flat. The oxidized wafers were then examined by AFM to determine the surface morphology.

C. Results

The morphology of the SiC was examined prior to oxide deposition. The range of root mean square (RMS) roughness values from AFM on cleaned substrates is 0.95nm to 1.36nm. These values served as the benchmark for determining whether or not the surface morphology of the deposited oxide was an issue for the quality of the oxides. The surface roughness of samples with and without tungsten sputtered on the backside (Fig. 1a & 1b) were nearly identical.

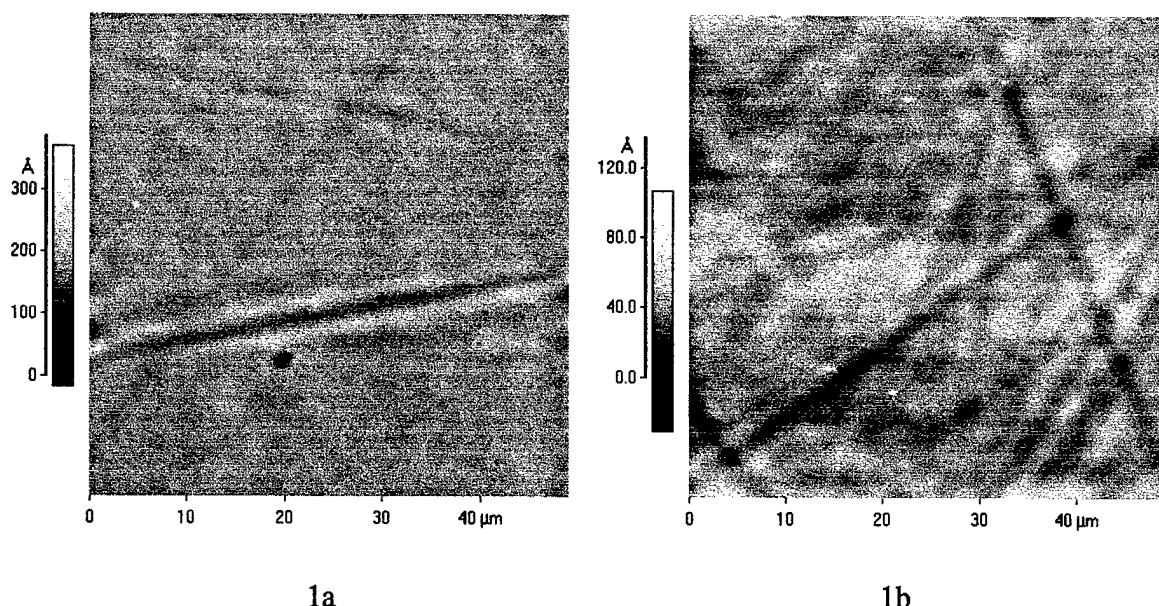


Figure 1. AFM of cleaned substrate (a) without tungsten on the backside, (b) with tungsten on the backside

The substrates with tungsten on the backside exhibited a RMS roughness of 1.13 nm; while the substrates without tungsten deposited on the backside showed a roughness of 1.87 nm. Since the RMS roughness between the two was less than 1 nm, it was resolved that the tungsten backside contact had little to no affect on the surface morphology of the sample.

The polishing scratches were very prevalent. The scratches were about 10 nm peak to valley on the cleaned wafers. The thermal oxide wafers showed little change from the cleaned wafers. The roughness of the thermal oxide samples is 0.93 nm (Fig. 2), and the peak to valley height of the scratches was still about 10 nm.

These polishing scratches were not removed by the sacrificial thermal oxidation and were a concern for gate dielectric quality. Furthermore, after an initial plasma oxidation, via O₂ or N₂O plasma, the morphology of the bare substrate and the initial plasma insulator were identical. The polishing scratches were too pronounced to be removed by a short plasma treatment or thermal oxidation.

Since PECVD oxides required the lowest thermal cycle, it may be a preferred process for gate oxide deposition. After a PECVD oxide deposition, the RMS surface roughness increased to between 2.1 to 2.3 nm. The roughness was reduced to 1.43 to 1.74 nm after a RTA (Fig. 3a & 3b).

A reduction of approximately 5 Å RMS roughness was observed after a 60 sec densification of the oxide at 1000C. The densified PECVD oxide roughness was essentially equivalent to the substrate roughness. The polishing scratches were also prevalent through the PECVD deposited films. The scratches were of the same depth as the cleaned substrates. Therefore, the PECVD densified oxide did not significantly change the surface morphology of the substrate, and did not lessen the depth of the polishing scratches.

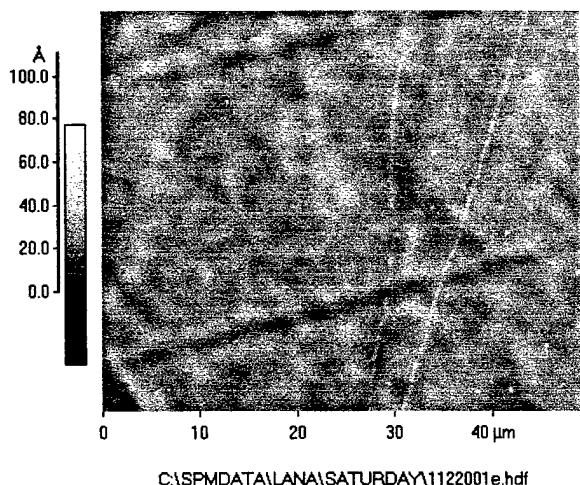


Figure 2. AFM of thermal oxide grown at 1050C for 2 hr.

Likewise, the LPCVD oxides (Figs. 4a & 4b) had RMS roughness of 2.55nm, which was slightly reduced to 1.99nm after RTA. Again, the densified oxide RMS roughness was essentially equivalent to the substrate roughness. The LPCVD films exhibited the same overall RMS roughness as the SiC wafer, and the polishing scratches were still prevalent, and undiminished.

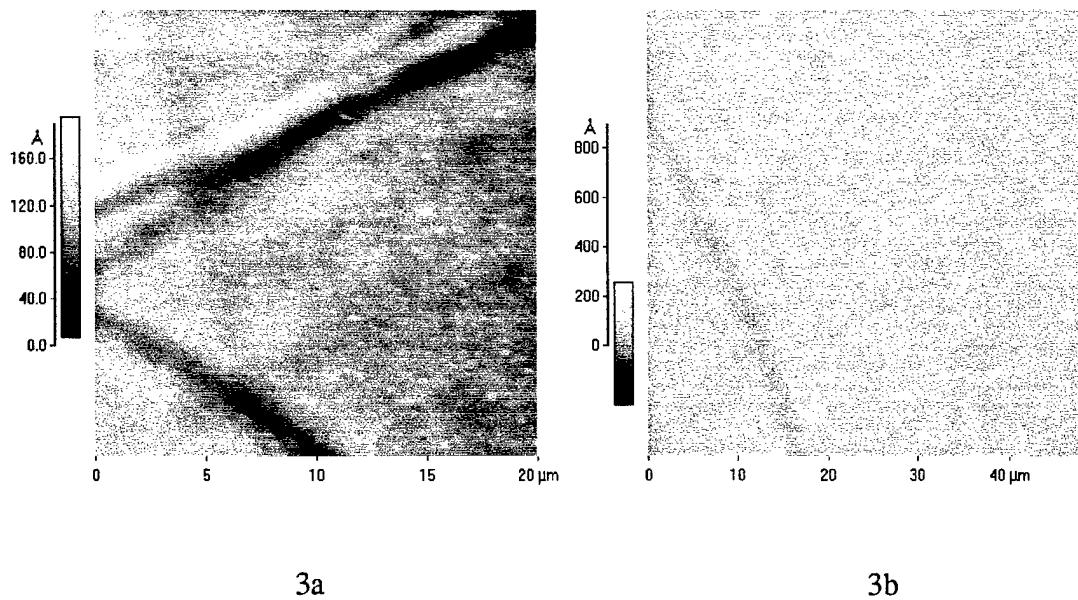


Figure 3. AFM of PECVD oxides (a) before RTA, (b) after RTA.

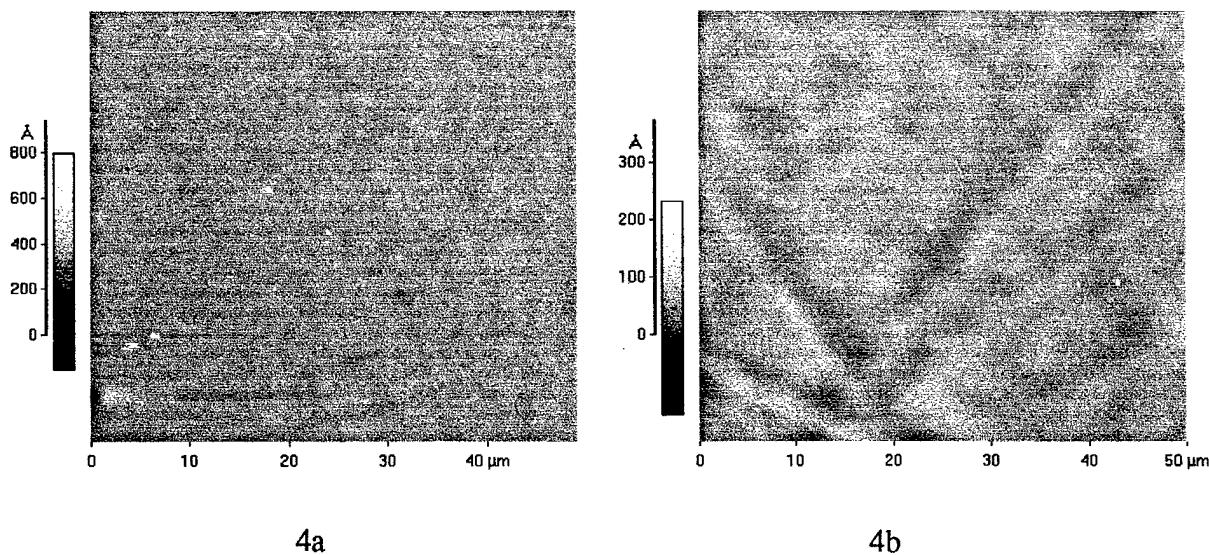


Figure 4. AFM of LPCVD Oxides (a) Before RTA, (b) after RTA.

LTO deposited oxides exhibited similar behavior (Figs. 5a & 5b). The LTO deposition process did not appear to roughen the surface morphology. The before and after RTA RMS roughness (1.38 nm and 1.02 nm, respectively) corresponded to the RMS values for the cleaned substrates. The LTO process was typically used as a final passivation layer. It was shown that the LTO process did not affect the depth and roughness of the polishing damage.

The LTO, PECVD, and LPCVD deposited oxides did not significantly increase the RMS roughness of the wafer surface. The polishing scratches were evident even after the oxide deposition or the thermal oxidation. The polishing scratches were still the most noticeable cause for surface roughness. The scratches were about 1/4 of the thickness of the gate dielectric. While the scratches were evident, the films deposited by PECVD, LPCVD, and LTO demonstrated that smooth surfaces may be obtained from a smooth starting surface. Therefore, deposited oxide morphology was expected to have little effect on the quality of the gate dielectric.

D. Conclusions

Deposited oxides on silicon carbide can be prepared without significantly increasing the surface roughness. The roughness is not significantly reduced by thermally oxidizing the wafer. For PECVD films, it was found that a 1 min rapid thermal anneal at 1000C is sufficient to lower the RMS roughness to within 1nm of the substrate roughness. With no significant roughening of the surface by PECVD or LPCVD of oxides on silicon carbide, deposited oxides may be a viable alternative to thermal oxidation for gate dielectrics. The morphology of

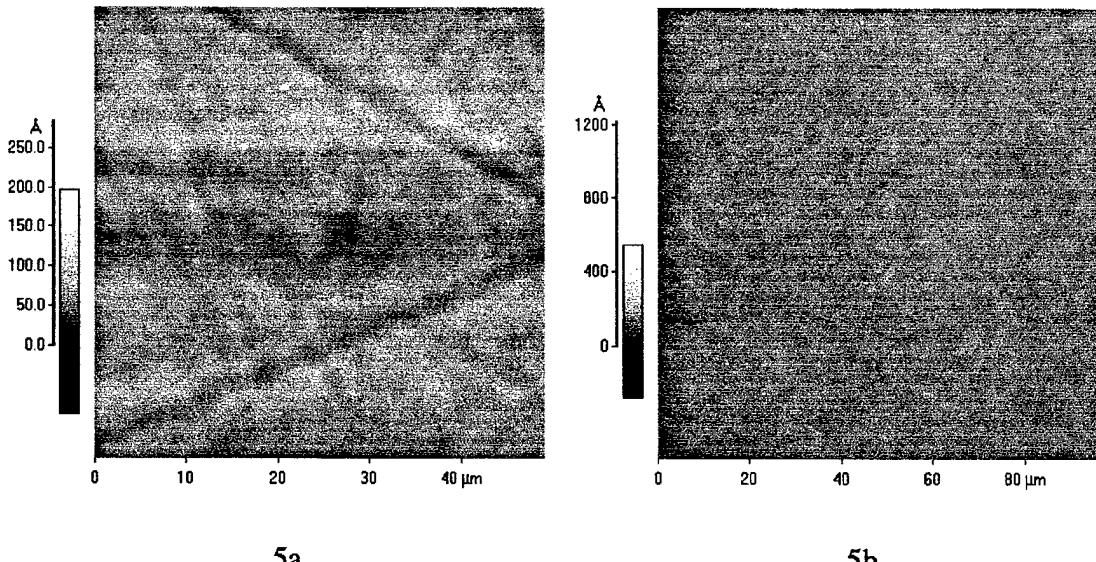


Figure 5. AFM of LTO (a) before RTA, (b) after RTA.

deposited oxides is expected to have little to no effect on electrical characteristics of devices on silicon carbide. However, the polishing techniques for silicon carbide need to be improved. The polishing scratches propagate through the epi-layer and the deposited and thermal oxides. The depth of these scratches is of the order of the gate thickness. The depth of the scratches must be reduced to assure a smooth surface for processing.

D. Future Work

Currently, capacitors are being fabricated for electrical testing. Both C-V and I-V testing will be performed to determine the quality of the oxide. Further depositions will be performed to attempt to improve the quality of the deposited oxides. Furthermore, examination of the SiO₂/SiC interface will be performed via ARUPS and XPS to determine the interface characteristics of the materials.

E. Acknowledgments

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